MASSEY UNIVERSITY
ENGINEERING

IEEE
IEEE NZ Central Section

Joint Massey University / IEEE NZ Central Section Workshop

Implementing Image Processing on FPGAs

Palmerston North
23-25 November, 2011

Course information:

About the course

Field Programmable Gate Arrays (FPGAs) are increasingly being used as an implementation platform for real-time image processing applications because their structure is able to exploit spatial and temporal parallelism. Unfortunately, simply porting an algorithm onto an FPGA often gives disappointing results, because most image processing algorithms have been optimised for a serial processor. Therefore it is necessary to transform the algorithm to efficiently exploit the parallelism inherent within the algorithm. This course introduces a design approach for FPGA based imaging system development, highlighting the significant differences between hardware and software based design. Through lectures and hands-on laboratories, the basic tools for FPGA based development are introduced, and used for implementing a range of image processing operations leading to a simple target tracking system.

Who should attend?

This course is aimed at engineers and scientists who need to understand basic concepts of FPGAs, and how they may be applied to image processing. It is targeted particularly for those who are entering this field, or are looking at using FPGAs for an image processing application. Participants are expected to have some background in basic electronics, mathematics, and programming. A basic understanding of image processing concepts would be helpful, although prior background in FPGAs is not required.

About the Presenter

Associate Professor Donald Bailey has over 30 years of experience in image processing and machine vision. Over the last 10 years he has conducted extensive research in mapping image processing algorithms onto FPGAs. He is the author of many publications in this field, including the book "*Design for Embedded Image Processing on FPGAs*."

Registration (Registrations close 28 October 2011. Please register early to avoid disappointment as places are limited)

Name: .....

Organisation: .....

Email address: .....

Registration includes course notes, lunches and refreshment during tea breaks

		IEEE member	non-member	Fee
Full Registration		$700	$900	
Student Registration		$300	$400	
Optional extras:	Terasic DE0 board and D5M camera*		$275	
Total due:				

* Boards will be provided at the course. This option is for you to purchase your board to keep. This is at cost and includes GST.

Payment details:

Credit card: VISA / Mastercard Card number: ..... Expiry (MM/YYYY): .....

Name on card: ..... Signature: ..... Date: .....

Fax completed form to (06)350 2259 or email scanned copy to D.G.Bailey@massey.ac.nz

Cheque: Make payable to **Massey University** and post to: Donald Bailey, School of Engineering and Advanced Technology, Massey University, Private Bag 11222, Palmerston North 4442.

Course Content:

Day 1:

- Image processing and FPGAs
- Introduction to VHDL
- Laboratory: Using Altera's Quartus tools / implementing a display driver
- Introduction to Handel-C
- Laboratory: Using Mentor Graphics' DK / development environment
- Image capture
- Laboratory: Image capture and display from DE0 & D5M

Day 2:

- Implementing filters: Colour filter array demosaicing, error diffusion
- Laboratory: Adding Bayer pattern filtering to camera and error diffusion to display
- Filters: Convolution and morphology
- Laboratory: Implementing Sobel filter, and CORDIC arithmetic
- Histogram processing
- Laboratory: Histogram display, and histogram equalisation

Day 3:

- FPGA based design and algorithm implementation
- Colour processing
- Laboratory: Colour detection
- Bounding box
- Laboratory: Implementing bounding box
- Laboratory: Closing the loop with tracking