IEEE EDS/MTT-S/SSCS
Youngnam Chapter Inauguration
Colloquia on

Nanotechnology
&
Nanodevices

일시: 2008년 5월 14일 (수요일) 오후 1시 30분 – 6시 30분
장소: 대구 EXCO
주최: IEEE EDS/MTT-S/EDS 영남 챕터
대한전자공학회
후원: 경북대학교 BK21 정보기술인력양성사업단
포항공과대학교 BK21 미래정보기술사업단
포항나노기술집적센터(NCNT)
IEEE EDS Korea 챕터
안내: 포항공과대학교 정 진용 교수 achung@postech.ac.kr

안녕하십니까?
IEEE EDS/MTT-S/SSCS 영남 챕터에서는 창립 기념으로, 나노기술 분야 전문가 다섯 분을 모시고, 대한전자공학회와 공동주최, 경북대학교 BK21 정보기술인력양성사업단, 포항공과대학교 BK21 미래정보기술사업단과 포항 나노기술집적센터(NCNT)및 IEEE EDS Korea 챕터 후원으로 오는 5월 14일 (수요일) 오후 1시 30분부터 대구엑스코에서 2008 춘계 한국전자전에서 공동 기조 연설을 가진 후, 세미나를 개최 합니다. 나노기술에 관하여 세계적인 권위를 가지신 분들의 강의가, 연구와 업무 수행에 많은 도움이 되기를 기대하겠습니다.

IEEE EDS/MTT-S/SSCS 영남 챕터 회장
포항공과대학교 전자전기공학과 교수 정 윤하 드림

기조 연설 순서 (13:30 – 14:50)

연사	소속	제목
Prof Takao Someya	**Univ. of Tokyo**	**Molecular Nanotechnology and Ubiquitous Electronics World**
Prof Soo-Young Lee	**KAIST**	**Artificial Brain: A Brain-Inspired Intelligent System Based on the Integration of Computational Neuroscience, Cognitive Science and Information Technology**

세미나 순서 (15:00 – 18:35)

연 사	소 속	제 목
Prof Takao Someya	**Univ. of Tokyo**	**Organic transistor integrated circuits: Towards ambient electronics**
Prof Moon-Ho Jo	**POSTECH**	**Bottom-up semiconductor nanowires: materials syntheses and device developments**
Prof Huei Wang	**National Taiwan University**	**Current Status and Future Trends for Si and Compound MMICs in Millimeter-Wave Regime and Related Issues for System on Chip (SoC) and/or System in Package (SiP)**
Prof Juin Liou	**Univ. of Central Florida**	**ESD Protection for nano CMOS devices**
Prof Jong Ho Lee	**Kyungpook National University**	**3-D Device Modeling of Double-Gate and Nanowire FETs**

Organic transistor integrated circuits: Towards ambient electronics

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Abstract

In the forthcoming ambient electronics era, multiple electronic objects are scattered on walls, ceilings or in imaginative locations and interact each other to enhance safety, security and convenience.

For implementation of many electronic objects in our daily life, large-area sheet-type devices are needed and organic transistors are expected to play an important role. In this talk, I will describe recent progress and future prospects of organic transistor-based flexible, large-area sensors and actuators, such as electronic artificial skins (e-skins) and wireless power transmission sheet.

Particularly, I will report on printed organic nonvolatile memory that has been developed to realize skin-like large-area interfaces.

About the Speaker

Takao Someya received the Ph.D. degree in electrical engineering from the University of Tokyo in 1997. In 1997, he joined Institute of Industrial Science (IIS), the University of Tokyo, as a Research Associate and was appointed to be a Lecturer of the Research Center for Advanced Science and Technology (RCAST), the University of Tokyo, in 1998, and an Associate Professor of RCAST in 2002. From 2001 to 2003, he worked for the Nanocenter (NSEC) of Columbia University and Bell Labs, Lucent Technologies, as a Visiting Scholar. Since 2003, he has been an Associate Professor of the Department of Applied Physics and Quantum-Phase Electronics Center, the University of Tokyo. His current research interests include organic transistors, flexible electronics, plastic integrated circuits, large-area sensors, and plastic actuators. Dr. Someya is a member of the IEEE Electron Devices Society, the Materials Research Society (MRS), and the Japanese Society of Applied Physics. He is an IEEE/EDS Distinguished Lecturer since 2004 and a recipient of 2004 IEEE/ISSCC Sugano Award. Dr. Someya's "large-area sensor array" electronic thin film was featured in Time Magazine as one of its "Best Inventions of 2005" in its November 21st issue.

Bottom-up semiconductor nanowires: materials syntheses and device developments

Moon-Ho Jo

Department of Materials Science and Engineering, Pohang University of Science and Technology (POSTECH),

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Abstract

Growth of bottom-up semiconductor nanowires (NWs) exploits the highly asymmetric growth kinetics in the radial and axial directions, and often effectively employs metal nanoparticles as liquid catalysts for the dimensionally confined nucleation and the subsequent one-dimensional crystal growth. In this talk, we present our recent developments of alternative NW growth schemes employing "solid catalysts" in stead, which can provide practical advantages for the potential large-area integrated growth. We first show the "deterministic" growth of Ge NWs with the uniform diameter distribution at sub-10 nm at 200 ^{o}C using Cu-catalysts. Second, we describe the "self-organized" growth of NiSi NWs, by which SiH_4 chemical vapor reacts with Ni thin films to spontaneously grow NiSi NWs. Third, we demonstrate vertical array growth of Si and Ge NWs in an epitaxial manner, from which we currently explore for the possible applications into Si optoelectronics. Finally we overview and discuss general implications of our NW growth methods for the large-area integrated device applications.

About the author

Personal Information

- **Associate Professor** (03/2008 -),
  Assistant Professor (01/2005 – 02/2008)
  Department of Materials Science and Engineering,
  Pohang University of Science and Technology (POSTECH), KOREA

Education

- **Postdoctoral Research Fellow** (10/2001 – 10/2004)
  Harvard University, Chemistry/Physics
  Research Areas: "Molecular electronics and Nano-electronics"
- **Ph.D.** (-9/2001)
  University of Cambridge, Materials Science
  Dissertation: "Spin-polarised tunnel junctions based on half-metallic manganites"
- **Visiting Scholar** (-8/1998)
  University of Tokyo, Electrical Engineering
- **M.S./B.S.** (-9/1997)

Yonsei University, Materials Science and Engineering

M.S. Thesis: "Syntheses and characterization of SiO_2 aerogel thin films as intermetal dielectrics for deep sub-micron Si-device applications"

Research interests

- Gas-phase syntheses of nanowires for nanoelectronics and nano- optoelectronic.s
- Fro a range of solid-state electronics, particularly,

1. Electron transport in low-dimensional systems such as semiconductor nanowires, quantum dots and single molecules.
2. Nanowire optoelectronics and photovoltaics.
3. Magnetoelectronics such as magnetic tunnel devices and magneto-electronic memories based on low-dimensional ferromagnetic metals.

Professional Affiliations

Member of American Physical Society
Member of Materials Research Society
Member of American Chemical Society
Member of Institute Of Physics

Professional ACTIVITIES

국가 나노기술로드맵 작성위원

국가 전략기술로드맵 기획위원 (나노소자)

Current Status and Future Trends for Si and Compound MMICs in Millimeter-wave Regime and Related Issues for System on Chip (SOC) and/or System in Package (SIP) Applications

The anticipated presentation will cover the current status and future trends of millimeter-wave MMICs, including those using III-V compound (GaAs, InP, GaN, etc.) and Si-based (CMOS, SiGe HBT and BiCMOS) MMIC technologies. Millimeter-wave MMICs used to be applied to military and astronomy systems for long time and started to be utilized for civil applications in the decade, such as communications and automotive radars. The evolution of IC technologies has enabled the performance of Si-based MMICs over 100 GHz, even in standard bulk CMOS processes. This is believed to have a major impact in the future development of millimeter-wave systems. Since low-cost mass-production potential pushes forward the technology, a very high integration of circuit functions on a chip, such as RF, base-band circuitry, automatic-control for a steady operation, and maybe even the antenna, etc. should be included, and thus the system on chip (SOC) issues should be addressed, especially in MMW regime. Moreover, millimeter-wave packaging cost always dominated in the module development. In order to simplify the assembly and reduced cost, the concept of system in package (SIP) has been proposed. This presentation will also survey the current technologies for SOC and SIP and discuss related issues and challenges.

Huei Wang (S'83-M'87-SM'95-F'06) was born in Tainan, Taiwan, Republic of China on March 9, 1958. He received the B. S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, Republic of China in 1980, and the M. S. and Ph. D. degrees in electrical engineering from Michigan State University, East Lansing, Michigan in 1984 and 1987, respectively.

During his graduate study, he was engaged in the research on theoretical and numerical analysis of electromagnetic radiation and scattering problems. He was also involved in the development of microwave remote detecting/sensing systems. Dr. Wang joined Electronic Systems and Technology Division of TRW Inc. since 1987. He has been an MTS and Staff Engineer responsible for MMIC modeling of CAD tools, MMIC testing evaluation and design and became the Senior Section Manager of MMW Sensor Product Section in RF Product Center. He visited the Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, in 1993 to teach MMIC related topics and returned to TRW in 1994. He joined the faculty of the Department of Electrical Engineering of National Taiwan University, Taipei, Taiwan, Republic of China, as a Professor in February 1998. He is currently the Director of Graduate Institute of Communication Engineering of National Taiwan University.

Dr. Wang is a member of the honor society Phi Kappa Phi and Tau Beta Pi. He received the Distinguished Research Award of National Science Council, ROC, at 2003. He was the Richard M. Hong Endowed Chair Professor of National Taiwan University in 2005-2007. He was elected as an IEEE Fellow in 2006, and has been appointed as an IEEE Distinguished Microwave Lecturer for the term of 2007-2009. Dr. Wang received the Academic Achievement Award from Ministry of Education, ROC, in 2007.

Electrostatic Discharge (ESD) Protection Solutions for Nano CMOS Technology

Juin J. Liou
Analog Devices Chair Professor
School of EE and CS, University of Central Florida, Orlando, Florida, USA
Cao Guang-Biao Endowed Professor
Dept. of ISEE, Zhejiang University, Hangzhou, China

Abstract

Electrostatic discharge (ESD) is a process in which a finite amount of charge is transferred from one object (i.e., human body) to the other (i.e., microchip). This process can result in a very high current passing through the microchip within a very short period of time, and more than 35% of chip damages can be attributed to such an event. As such, designing robust on-chip ESD structures to protect microchips against the ESD stress is a high priority in the semiconductor industry. An overview on the ESD sources, models, and protection schemes will first be given in this talk. This is followed by the examples of robust ESD protection solutions designed for nano CMOS technology including the 180-nm data communication transceiver, 90-nm gas-sensor system-on-chip, and 65-nm radio frequency IC.

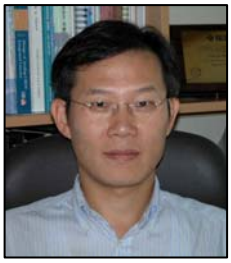
Biography of Juin J. Liou

Juin J. Liou received the B.S. (honors), M.S., and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1982, 1983, and 1987, respectively. In 1987, he joined the Department of Electrical and Computer Engineering at the University of Central Florida, Orlando, Florida where he is now a Professor. His current research interests are Micro/nanoelectronics computer-aided design, RF device modeling and simulation, and electrostatic discharge (ESD) protection design and simulation.

Dr. Liou has been awarded 3 U.S. patents (3 more filed and pending), and has published 8 books, more than 220 journal papers (including 14 invited articles), and more than 160 papers (including 58 keynote or invited papers) in international and national conference proceedings. He has been awarded more than $8.0 million of research contracts and grants from federal agencies (i.e., NSF, DARPA, Navy, Air Force, NIST), state government, and industry (i.e., Semiconductor Research Corp., Intel Corp., Intersil Corp., Lucent Technologies, Alcatel Space, Conexant Systems, Texas Instruments, Fairchild Semiconductor, Analog Devices, RF Micro Device, Lockheed Martin), and has held consulting positions with research laboratories and companies in the United States, China, Japan, Taiwan, and Singapore. In addition, Dr. Liou serves as a technical reviewer for various journals and publishers, general chair or technical program chair for a large number of international conferences, and regional editor (in USA, Canada and South America) for the *Microelectronics Reliability* journal.

Dr. Liou received ten different awards on excellence in teaching and research from the University of Central Florida (UCF) and six different awards from the IEEE Electron Device Society. Among them, he was awarded the UCF Distinguished Researcher Award three times (1992, 1998, 2002), UCF Research Incentive Award two times (2000, 2005), UCF Analog Devices Chair Professor (2008), and IEEE Joseph M. Biedenbach Outstanding Engineering Educator Award in 2004 for his exemplary teaching, research, and international collaboration. His other honors include Fellow of the Institute of Electronic Engineers (IEE), IEEE Electron Device Society (EDS) Distinguished Lecturer, National Science Council Distinguished Lecturer, Yangtze River Scholar Endowed Chair Professor – the highest honorary professorship in China, Cao Guang-Biao Endowed Professor of Zhejiang University, China, Consultant Professor of Huazhong University of Science and Technology, Wuhan, China, and Courtesy Professor of Shanghai Jiao Tong University, Shanghai, China. Dr. Liou was a recipient of U.S. Air Force Fellowship Award and National University Singapore Fellowship Award.

Dr. Liou served as the IEEE EDS Vice-President for Regions/Chapters, IEEE EDS Treasurer, IEEE EDS Finance Committee Chair, IEEE EDS Administrative Committee Elected Member, and IEEE EDS Educational Activities Committee Member.



3-D Device Modeling of Double-Gate and Nanowire FETs

Jong-Ho Lee, Professor

Kyungpook National University

ABSTRACT

The threshold voltages (V_{th}) of the double/triple-gate bulk FinFETs implemented on bulk silicon wafers were modeled systematically and compared with data obtained from 2-D or 3-D device simulation. The V_{th} modeling of the bulk FinFETs was performed by considering charge-sharing, top corner effect, and surface potential lowering. The model predicted the V_{th} behavior with fin body thickness, body doping concentration, gate length, gate height, and corner shape of the fin body well. Our compact model made an accurate V_{th} prediction of the devices with the gate length up to 20 nm and the fin body width up to 5 nm. The diffusion and drift currents of fully depleted symmetric double-gate (DG) MOSFETs with doped-channel were physically modeled with the simple closed-form based on the charge-sheet approximation. Also, the threshold voltage modeling of DG MOSFETs by considering drain bias (VDS) was performed simply based on surface potential and diffusion current model. In this work, our compact models predicted accurately DC characteristics of the devices with the channel length (L) to 20 nm and shown good agreement with 2-D simulation. We introduce the modeling of the surface potential and diffusion current of surrounding gate (SG) MOSFETs with doped channel in the subthreshold region. Our compact model are verified in terms of channel length, fin body width, and body doping concentration at a given VGS and VDS by comparing with the results of the 3-D device simulation, and shown a good agreement with 3-D simulation.

About the author

“Jong-Ho Lee”, Ph.D. has been a full professor at Kyungpook National University since 2002 with lecture and research. He has been working for National Education Center for Semiconductor Technology as deputy director since 2003, and working for Semiconductor Fusion Technology Center as lab supervisor. He has authored or coauthored 90 journal papers and over 189 conference papers related to his research area, and has been granted 51 patents in the area. He invented bulk FinFETs and various flash memory devices based on the bulk FinFET structure. He also invented Saddle FinFETs (or Saddle MOSFETs) which is very promising in sub-50 nm DRAM cell technology, 2-bit/cell or 4-bit/cell NOR flash memory cell based on recess channel structure, and high-density/high-performance NAND flash string in which cells have no source/drain and/or low-interference/high-coupling-ratio storage electrode. In 2006, he was a recipient of the “This Month’s Scientist Award” for his contribution in the development of practical high-density/high-performance 3-dimensional nano-scale CMOS devices.

Prior to joining Kyungpook National University, “Prof. Lee” was a professor at Wonkwang University. He was also with ETRI as an invited member of technical staff. During his 4 years at ETRI, “Prof. Lee” spent time doing device design/characterization of CMOS devices, 1/f noise and device mismatch analysis for IC design. From August 1998 to July 1999, he worked at MIT as a post-doctor, where he was engaged in the research on sub-100 nm double-gate CMOS devices.

”Prof. Lee” received a B.S. degree in Electronic Engineering from Kyungpook National University, Daegu, Korea, and M.S. and Ph.D degrees in Electronic Engineering from Seoul National University, Seoul, Korea. His research interests include sub-100 nm CMOS and flash memory technologies, device characterization and modeling for RF application, analog IC design for intelligent sensors, and 3-D Microsystems including sensors. Prof. Lee is now affiliated with Kyungpook National University.